Amendments to the Claims

The claims are unamended. The currently pending claims are listed below.

1. (Previously Presented) A method of eliminating parasitic bipolar transistor action in a Silicon on Insulator (SOI) Metal Oxide Semiconductor (MOS) device located in a logic circuit, said logic circuit being adapted to receive an input signal and a clock signal, the method comprising:

controlling the conduction of an active discharging device with the input signal, said active discharging device being coupled to an intermediate node of said logic circuit, whereby the parasitic bipolar transistor is deactivated.

2. (Previously Presented) The method of claim 1, wherein the SOI device comprises a gate and a drain, and wherein the method further comprises:

providing a first signal to said gate of said SOI device;

providing a second signal to said drain of said SOI device; and

activating the conduction of said active discharging device according to the state of said first signal.

3. (Previously Presented) The method of claim 2 wherein the first signal is said input signal.

4. (Previously Presented) The method of claim 2 wherein said first signal causes said SOI device to conduct current whenever said logic circuit is being pre-charged.

5. (Previously Presented) The method of claim 2 wherein the second signal pre-charges said drain during a pre-charge cycle.

6. (Previously Presented) The method according to claim 1, wherein the active discharging device provides a conduction path between said intermediate node and a voltage source.

7. (Previously Presented) A method of eliminating parasitic bipolar transistor action in a Silicon on Insulator (SOI) Metal Oxide Semiconductor (MOS) dynamic logic circuit having an input, an output, a clock, an active discharge transistor, and a plurality of stacked SOI Metal Oxide Semiconductor (MOS) transistors interconnected to define a common node and an intermediate node, wherein:

said plurality of stacked SOI MOS transistors is controlled by a plurality of inputs;

said common node is coupled to a pre-charging device;

said intermediate node is in a path between said common node and a voltage source, said path defined by said plurality of stacked SOI MOS transistors;

said intermediate node is coupled to said common node by at least a first of said plurality of stacked SOI MOS transistors; and

said active discharging transistor is controlled by at least one of said plurality of inputs, said active discharging transistor defining a discharge path between said intermediate node and said voltage source,

the method comprising:

controlling the conduction of said active discharging transistor during a pre-charge cycle; and

actively discharging said intermediate node, whereby the parasitic bipolar transistors are deactivated and the charge at said intermediate node is maintained at a predetermined level.

8. (Original) The method according to claim 7, wherein pre-charging occurs during a low state of said clock.

9. (Original) The method according to claim 7, wherein pre-charging occurs during a high state of said clock.

10. (Original) The method according to claim 7, wherein during the pre-charging all said inputs are set to a predetermined logic state.

11. (Original) The method according to claim 10, wherein said logic state is low.

12. (Original) The method according to claim 10, wherein said logic state is high.

13. (Original) The method according to claim 7, wherein the step of actively discharging said intermediate nodes prevents the body voltages of said stacked SOI transistors from reaching a voltage stage sufficient to activate the parasitic bipolar transistors of said stacked SOI transistors.

14. (Original) The method according to claim 7, wherein said stacked transistors are N-Field Effect Transistors (NFET) and said active discharging transistors are P-Field Effect Transistors (PFET).

15. (Original) The method according to claim 7, wherein said stacked transistors are P-Field Effect Transistors (PFET) and said active precharging transistors are N-Field Effect Transistors (NFET).

16. (Original) The method according to claim 7, wherein said pre-charging device comprises transistors coupled to said stacked transistors.

17. (Previously Presented) A method of reducing the effects of parasitic bipolar transistor action in a silicon-on-insulator (SOI) logic circuit during a pre-charge cycle, comprising:

coupling an active discharge device to an intermediate node of the SOI logic circuit; and

controlling the conduction of the active discharging device using a non-clock signal, whereby the charge at the intermediate node is maintained at a predetermined level during the pre-charge cycle.

18. (Previously Presented) The method of claim 17, wherein the predetermined level is a common ground potential for the SOI logic circuit.

19. (Previously Presented) The method of claim 17, wherein the non-clock signal comprises an active low signal applied to an input of the SOI logic circuit during the pre-charge cycle.

20. (Previously Presented) The method of claim 1, wherein said input signal is a non-clock signal.

21. (Previously Presented) The method of claim 6, wherein the voltage source comprises a system ground.